




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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,906	09/30/2003	Jason MacNeal	AVX-236	9002
22827	7590	09/03/2004	EXAMINER	
DORITY & MANNING, P.A. POST OFFICE BOX 1449 GREENVILLE, SC 29602-1449			THOMAS, ERIC W	
			ART UNIT	PAPER NUMBER
			2831	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/674,906	<b>Applicant(s)</b> MACNEAL ET AL.	
	<b>Examiner</b> Eric W Thomas	<b>Art Unit</b> 2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 May 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-5,10,11,15-18,22-26,30 and 31 is/are rejected.
- 7) ☒ Claim(s) 2, 6-9, 12-14, 19-21, 27-29, 32-34 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 5/10/04 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>5/04</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Specification***

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Applicant uses "comprises" in the abstract.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Claim Objections***

3. Claim 33 is objected to because of the following informalities:

Claim 33 is confusing. The examiner believes that this claim should depend on claim 32.

Appropriate correction is required.

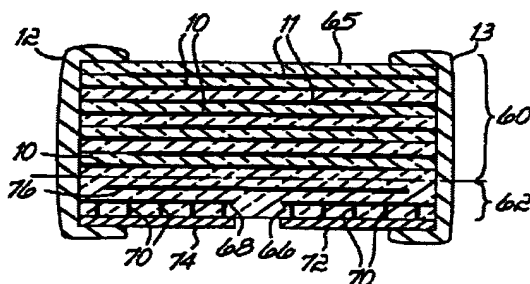
**Claim Rejections - 35 USC § 102**

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 5, 11, 23, 26, 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Devoe et al (US 6,587,327).



Devoe et al. disclose in fig. 9A, a multilayer electronic device, comprising: a plurality of dielectric layers; a plurality of electrode layers (10,11) interleaved with selected of said plurality of dielectric layers to form a multilayered arrangement, said multilayered arrangement defined by first and second opposing surfaces and a plurality of side surfaces; at least one respective first (68) and second (66) transition layer electrode portion provided on the first surface of said multilayered arrangement; a cover layer (lower most ceramic layer) provided over said at least one respective first and second transition layer electrode portion, said cover layer formed to define a plurality of openings there

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through for exposing a portion of said at least one respective first and second transition layer electrode portions; at least one first peripheral termination formed along selected side surfaces of the multilayered arrangement and electrically connecting selected of said electrode layers and said at least one first transition layer electrode portion; and at least one second peripheral termination formed along selected side surfaces of the multilayered arrangement and electrically connecting selected of said electrode layers and said at least one second transition layer electrode portion.

Regarding claim 5, Devoe et al. disclose a plurality of via termination formed in the openings defined by the covering.

Regarding claim 11, Devoe et al. disclose said at least one first and second peripheral terminations extend along a substantially entire dimension of a respective selected side surface of the multilayer electronic device and wrap around to at least one surface adjacent to said respective selected side surface.

Regarding claim 22, Devoe et al. disclose said at least one first and second peripheral terminations extend along a substantially entire dimension of a respective selected side surface of the multilayer electronic device and wrap around to at least one surface adjacent to said respective selected side surface.

Regarding claim 23, Devoe et al. disclose a multilayer capacitor, comprising: a plurality of first layers (11 & dielectric), each first layer having a sheet of dielectric material delimited laterally by edges and partially covered by a first electrode plate; a plurality of second layers, each second layer (10 & dielectric) having a sheet of dielectric material delimited laterally by edges and

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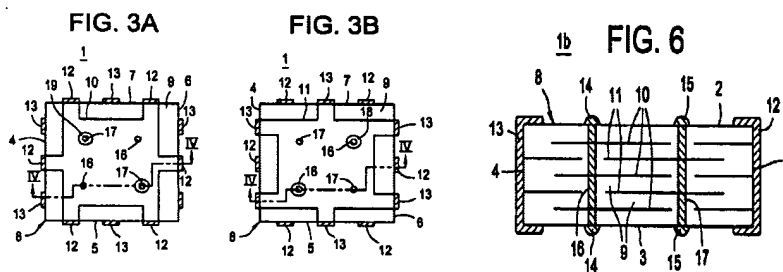
partially covered by a second electrode plate; said first and second layers alternately stacked in a multilayered assembly such that adjacent first and second electrode plates form opposing capacitor plates, said multilayered assembly characterized by first and second opposing surfaces and a plurality of side surfaces; a transition layer (66,68 & dielectric) comprising a sheet of dielectric material and at least one respective first (66) and second (68) transition layer electrode portion provided on the sheet of dielectric material, said transition layer provided on the first surface of said multilayered assembly; and a cover layer provided over said transition layer, said cover layer formed to define a plurality of openings there through for exposing a portion of said at least one respective first and second transition layer electrode portions; wherein said first electrode plates and said at least one first transition layer electrode portion are exposed along selected side surfaces of the multilayered assembly in at least one substantially linear alignment such that said first electrode plates and said at least one first transition layer electrode portion are connected by at least one first peripheral termination (13); and wherein said second electrode plates and said at least one second transition layer electrode portion are exposed along selected side surfaces of the multilayered assembly in at least one substantially linear alignment such that said second electrode plates and said at least one second transition layer electrode portion are connected by at least one second peripheral termination (12).

Regarding claim 26, Devoe et al. disclose a plurality of via terminations formed in the openings defined by the cover layer.

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Regarding claim 31, Devoe et al. disclose the at least one first and second peripheral terminations extend along a substantially surface of the multilayer capacitor and wrap around to at least one surface adjacent to the said respective selected side surface.

6. Claims 15-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Kuroda et al. (US 6,594,136).



Kuroda et al. disclose in fig. 3A, 3B, 4, 9, a multilayer capacitor, comprising: a plurality of dielectric layers (9); respective pluralities of first (10) and second (11) electrode layers interleaved with selected of said plurality of dielectric layers to form a multilayered assembly, said multilayered assembly defined by topmost and bottommost layers and a plurality of adjacent side surfaces; at least one first via termination (16) provided through the topmost layer of said multilayered assembly and electrically connected to one of said first electrode layers; at least one second (17) via termination provided through the topmost layer of said multilayered assembly and electrically connected to one of said second electrode layers; at least one first peripheral termination (13) provided along selected side surfaces of said multilayered assembly and electrically connecting said plurality of first electrode layers; and at least one second peripheral termination (12) provided along selected side surfaces of said

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multilayered assembly and electrically connecting said plurality second electrode layers.

Regarding claim 16, Kuroda et al. disclose each of said plurality of first electrode layers respectively includes a plurality of electrode tabs extending to and exposed along selected side surfaces of said multilayered assembly, wherein said at least one first peripheral termination electrically connects selected electrode tabs from the plurality of first electrode layers, and wherein said at least one second peripheral termination electrically connects selected electrode tabs from the plurality of second electrode layers.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of



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35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuroda et al. (US 6,594,136).

Regarding claim 17, Kuroda et al. disclose the claimed invention except for the bottommost layer of the multilayer assembly comprise multiple <sup>of</sup> ~~of~~ the plurality of dielectric layers. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple dielectric layers on the bottommost layer of the multilayer assembly, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 3 USPQ 8.

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Regarding claim 18, Kuroda et al. disclose the claimed invention except for a plurality of solder balls connected to the at least one first via termination and to the at least one second via termination. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the via terminal from a solder material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

10. Claims 3-4, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devoe et al (US 6,587,327).

Regarding claims 3 & 24, Devoe et al. disclose the claimed invention except for the at least one respective first and second transition layer electrode

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portions are generally U-shaped or rectangular-shaped. It would have been an obvious matter of design choice to form the first and second transition layer electrode portions to have a rectangular-shape, since such a modification would have involved a mere change in the shape of a component, a change of shape is generally recognized as being within the level of ordinary skill in the art. *Span-Deck Inc. V. FabCon, Inc.*, 215 USPQ 835.

Regarding claims 4, & 25, Devoe et al. disclose the claimed invention except for the second surface of the multilayered arrangement comprises multiple of the plurality of dielectric layers.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple dielectric layers on the second surface of the multilayer assembly, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 3 USPQ 8.

Regarding claims 10, and 30, Devoe et al. disclose the claimed invention except for selected of the electrode layers and said at least one respective first and second transition layer electrode portions comprising ruthenium oxide such that the multilayer electronic device is characterized by a predetermined amount of equivalent series resistance.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form all the electrodes layers and the at least one respective first and second transition layer electrode portions from ruthenium oxide, since it has been held to be within the general skill of a worker in the art to

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select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

### ***Double Patenting***

11. Applicant is advised that should claim 11 be found allowable, claim 22 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof.

When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

### ***Allowable Subject Matter***

12. Claims 2, 6-9, 12-14, 19-20, 27-29, 32-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or fairly suggest (taken in combination with the other claimed features) a multilayer electronic device having at least one first and second transition layer electrode portions include a plurality of electrode tabs extending to and exposed along selected side surfaces of the multilayer arrangement (claim 2); a plurality of solders balls connected to selected of the plurality of via terminations (claim 6); the plurality of vias terminations comprises a second layer of resistor-polymeric material and a third

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layer of metallic material (claim 7); the plurality of via terminations comprise multiple layers of different metallic layer (claim 8); the at least one first and second transition layer electrode portions are plated directed to the exposed electrode portions (claim 9); an additional transition layer comprising a sheet of dielectric material and at least one respective additional first and second transition layer electrode portion (claim 12-14); selected of the at least one first via termination, at least one second via termination comprises a second layer of resistor-polymeric material and a third layer of metallic material (claim 19); selected of the at least one first via termination, and the at least one second via termination comprise multiple layers of different metallic layers (claim 20); a plurality of solder balls connected to selected of the plurality of via termination (claim 27); a plurality of solders balls connected to selected of the plurality of via terminations (claim 28); the plurality of vias terminations comprises a second layer of resistor-polymeric material and a third layer of metallic material (claim 29); and an additional transition layer comprising a sheet of dielectric material and at least one respective additional first and second transition layer electrode portion (claim 32-34).

***Conclusion***

In order to ensure full consideration of any amendments, affidavits, or declaration, or other documents as evidence of patentability, such documents must be submitted in response to this Office action. Submissions after the next Office action, which is intended to be a final action, will be governed by the requirements of 37 CFR 1. 116 which will be strictly enforced.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6,519,134 – disclose a capacitor having a terminal that connects to a printed circuit board

6,462,933 – disclose a thin film multilayer capacitor comprising a cover.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on M,Tu,Sat 9 am - 9:30 pm; W, Th, F 6 pm -10:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

 8/21/04

Eric W Thomas  
Examiner  
Art Unit 2831

ewt